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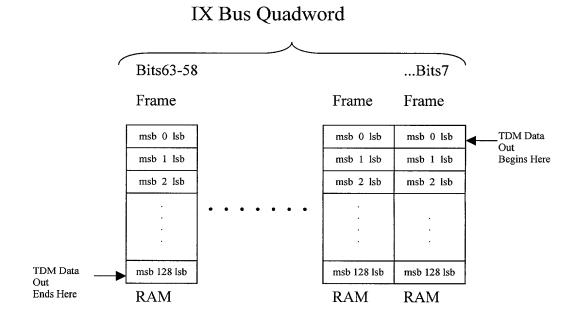


FIG. 19

4.1

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RAM4	RAM3		RAM2		RAM1		RAM0		_
Spare RAM Bank	F r a m e	HWY0							

FIG. 20